Abstract

The method and apparatus presented are targeted to improve the performance of moving data between memory portions connected by a system bus where writes have higher performance than reads, such as the PCI bus. Due to the PCI bus design, read requests from memories connected across the PCI bus take a significantly longer time to complete than performing a write operation under the same circumstances. The present invention uses the faster write operations across the PCI bus, and queue management techniques, to take advantage of the relative speed of writes in a PCI system. The overall result is significant performance enhancement, which is especially useful in service aware networks (SAN) where operation at wired-speed is of paramount importance.